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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/915,366 | 07/27/2001 | Yasuhito Suzuki | 50090-309 | 6983 |

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| EXAMINER |
|---|
| VU, QUANG D |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 12/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/915,366 | SUZUKI ET AL. | |
| | Examiner | Art Unit | |
| | Quang D Vu | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,886,408 to Ohki et al.

Regarding claim 1, Ohki et al. (figure 22) teach a semiconductor package comprising:

a die pad (a supporting layer under the chip [232-3]);

a die (232-3) mounted on the die pad (a supporting layer under the chip [232-3]);

a sealing member (resin package [235]) sealing therein the die (232-3), the bonding wires, parts of the outer leads (237) and a part of the die pad (a supporting layer under the chip [232-3]), and having an upper surface on the side of the die (232-3) and a lower surface on the side of the die pad;

wherein the outer leads (237) have upper electrical connecting surfaces on the side of the upper surface of the sealing member (an upper portion of the resin package [235]), and lower electrical connecting surfaces on the side of the lower surface of the sealing member (an upper portion of the resin package [235]), respectively, and the outer leads (237) have a height from a plane including the lower surface of the sealing member (an upper portion of the resin package

[235]) greater than that of the upper surface of the sealing member (an upper portion of the resin package [235]) from the same plane.

Since a plurality of outer leads (237) electrically connected to the thin film multi-layer circuit board 231 by bonding wires and the dies (232-3) electrically connected to the thin film multi-layer circuit board 231 by the external electrodes, the plurality of outer leads (237) electrically connected to the external electrodes of the die by bonding wires, respectively.

Regarding claim 2, Ohki et al. teach the upper electrical connecting surfaces of the outer leads (237) formed on the side of the upper surface of the sealing member (an upper portion of the resin package [235]) lie outside a projection region of the upper surface of the sealing member (an upper portion of the resin package [235]).

Regarding claim 4, Ohki et al. teach the outer leads (237) are formed in an L-shape (see figure 22).

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3 and 5-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,886,408 to Ohki et al.

Regarding claim 3, Ohki et al. teach the sealing member has four sides (column 14, lines 38-40). Ohki et al. differ from the claimed invention by not showing the outer leads are formed

on the four sides of the sealing member. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the outer leads are formed on the four sides of the sealing member because they increase the number of external connections between the die and the external circuit.

Regarding claim 5, Ohki et al. (figure 22) teach a semiconductor device, comprising:

a printed wiring board (257); and

a die pad (a supporting layer under the chip [232-3]);

a die (232-3) mounted on the die pad (a supporting layer under the chip [232-3]);

a sealing member (resin package [235]) sealing therein the die (232-3), the bonding wires, parts of the outer leads (237) and a part of the die pad (a supporting layer under the chip [232-3]), and having an upper surface on the side of the die (232-3) and a lower surface on the side of the die pad;

wherein the outer leads (237) have upper electrical connecting surfaces on the side of the upper surface of the sealing member (an upper portion of the resin package [235]), and lower electrical connecting surfaces on the side of the lower surface of the sealing member (an upper portion of the resin package [235]), respectively, and the outer leads (237) have a height from a plane including the lower surface of the sealing member (an upper portion of the resin package [235]) greater than that of the upper surface of the sealing member (an upper portion of the resin package [235]) from the same plane.

Since a plurality of outer leads (237) electrically connected to the thin film multi-layer circuit board 231 by bonding wires and the dies (232-3) electrically connected to the thin film

multi-layer circuit board 231 by the external electrodes, the plurality of outer leads (237) electrically connected to the external electrodes of the die by bonding wires, respectively.

Ohki et al. differ from the claimed invention by not showing a plurality of semiconductor packages, stacked up on the printed wiring board with outer leads included therein. It would have been obvious to one having ordinary skill in the art at the time the invention was made for a plurality of semiconductor packages, stacked up on the printed wiring board with outer leads included therein because a plurality of similar devices may be used to form a desired circuit on a printed wiring board. It has been held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced.

Regarding claim 6, Ohki et al. teach the upper electrical connecting surfaces of the outer leads (237) formed on the side of the upper surface of the sealing member (an upper portion of the resin package [235]) lie outside a projection region of the upper surface of the sealing member (an upper portion of the resin package [235]).

Regarding claim 7, Ohki et al. teach the sealing member has four sides (column 14, lines 38-40). Ohki et al. differ from the claimed invention by not showing the outer leads are formed on the four sides of the sealing member. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the outer leads are formed on the four sides of the sealing member because they increase the number of external connections between the die and the external circuit.

Regarding claim 8, Ohki et al. teach the outer leads (237) are formed in an L-shape (see figure 22).

Regarding claim 9, Ohki et al. (figure 22) teach a semiconductor device comprising:

a printed wiring board (257),

a die pad (a supporting layer under the chip [232-3]),

a die (232-3) mounted on the die pad (a supporting layer under the chip [232-3]);

a sealing member (resin package [235]) sealing therein the die (232-3), the bonding wires, parts of the outer leads (237) and a part of the die pad (a supporting layer under the chip [232-3]), and having an upper surface on the side of the die (232-3) and a lower surface on the side of the die pad;

wherein the outer leads (237) have upper electrical connecting surfaces on the side of the upper surface of the sealing member (an upper portion of the resin package [235]), and lower electrical connecting surfaces on the side of the lower surface of the sealing member (an upper portion of the resin package [235]), respectively, and the outer leads (237) have a height from a plane including the lower surface of the sealing member (an upper portion of the resin package [235]) greater than that of the upper surface of the sealing member (an upper portion of the resin package [235]) from the same plane.

Since a plurality of outer leads (237) electrically connected to the thin film multi-layer circuit board 231 by bonding wires and the dies (232-3) electrically connected to the thin film multi-layer circuit board 231 by the external electrodes, the plurality of outer leads (237) electrically connected to the external electrodes of the die by bonding wires, respectively.

Ohki et al. differ from the claimed invention by not showing a plurality of semiconductor packages mounted on the printed wiring board, each semiconductor package having an upper surface of a sealing member thereof facing the printed wiring board. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a plurality of

semiconductor packages mounted on the printed wiring board, each semiconductor package having an upper surface of a sealing member thereof facing the printed wiring board because a plurality of similar devices may be used to form a desired circuit on a printed wiring board. It has been held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced.

It is inherent that the outer leads of each of the packages connected to electrodes formed on the printed wiring board.

Regarding claim 10, Ohki et al. teach the upper electrical connecting surfaces of the outer leads (237) formed on the side of the upper surface of the sealing member (an upper portion of the resin package [235]) lie outside a projection region of the upper surface of the sealing member (an upper portion of the resin package [235]).

Regarding claim 11, Ohki et al. teach the sealing member has four sides (column 14, lines 38-40). Ohki et al. differ from the claimed invention by not showing the outer leads are formed on the four sides of the sealing member. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the outer leads are formed on the four sides of the sealing member because they increase the number of external connections between the die and the external circuit.

Regarding claim 12, Ohki et al. teach the outer leads (237) are formed in an L-shape (see figure 22).

Regarding claim 13, Ohki et al. teach the heat sink (236) constitutes the heat radiating passage above the circuit board (see figure 22). Ohki et al. differ form the claimed invention by not showing the die pad of the semiconductor package is provided on is exposed surface with a

cooling fin. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the die pad of the semiconductor package is provided on is exposed surface with a cooling fin because it depends on the amount of heat that dissipated from the die.

### *Response to Arguments*

Applicant's arguments with respect to claim 9 have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

qv
December 30, 2002

Steven Loke